International Journal on Emerging Technologies **10**(4): 354-358(2019)

ISSN No. (Print): 0975-8364
ISSN No. (Online): 2249-3255

Efficiency of Buck DC-DC Switching Power Converter in CCM and SDCM of Operation

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(Received 07 September 2019, Revised 08 November 2019, Accepted 18 November 2019)
(Published by Research Trend, Website: www.researchtrend.net)

ABSTRACT: This paper presents an efficiency comparison of buck DC-DC switching power converter in continuous current mode (CCM) and in synchronous discontinuous current mode (SDCM) of operation. Non-isolated synchronous buck DC-DC switching power converter is considered for this study. The circuit is made to operate in CCM and SDCM of operation, which depends on inductor value of the converter. SDCM of operation occurs when the circuit inductor value is smaller than critical inductor value and CCM of operation occurs when the circuit inductor value is larger than critical inductor value. CCM of operation has the advantage of less inductor current ripple. But it increases the inductor size, cost, weight and converter size. SDCM of operation have many advantages like the inductor size, cost, weight and converter size can be minimized. Also minimum turn-on loss, low diode reverse recovery loss, minimum inductor current parasitic ringing effect, and high power density are achieved. But it has large turn-off loss and increases inductor current ripple. Minimizing power loss across the power circuit for maximum efficiency is in current demand for industrial and other applications, and identifying optimum value of inductor and snubber capacitor for maximum efficiency, to minimum size, weight and cost is a challenging task. A series of MATLAB scripts are executed to find inductor value for SDCM and CCM of operation and to select snubber capacitor for maximum efficiency.

Keywords: Buck, CCM, Efficiency, Non-isolated, MATLAB scrip, SDCM.

I. INTRODUCTION

DC-DC switching power converters are power electronic circuits and by switching action it convert one level of electrical voltage into another level. These converters are used in number of fields like telecommunication, Uninterrupted Power Supplies (UPS), aerodynamics, DC machine drives, hybrid electric and fuel cell vehicles [1, 2], renewable energy system etc. The main task of a DC-DC converter is to produce a stable DC output voltage from a given input voltage. The converter is generally needed to control the DC load voltage produce a range of load currents drawn and/or range of input voltage applied. Preferably the DC output is to be noise less, that is current or voltage variation should be held below a specified level. In addition, the load energy is to be conveyed from the source with few set out level of efficiency. Power inductor choosing is a main step to attain these aims. Inductor value is determined to give a certain minimum amount of power storage and to decrease output current variation. Using the inductor value less than the calculated value produce more AC ripple on the DC output. Using much larger or much smaller inductor may cause the converter to switch between discontinuous and continuous modes of operation. A minimum inductor value causes a fast transient response; it also generates large current ripple, which produces more conduction losses in the switches, inductor, and parasitic resistances. The minimum inductor value requires a larger filter capacitor to minimize the output voltage ripple [3]. Switch turn-off loss and inductor current parasitic ringing effect are the main issues in SDCM of operation [4, 5]. These two issues are overcome by using snubber capacitor across each switch and by applying complementary gating signal control scheme. When a switch open, circuit parasitic inductor produce a voltage spikes which are removed by using snubber capacitor. Design process of snubber circuit for DC-DC converter and six topologies of snubber circuits were investigated in simulation tests [6]. Before the switch is turned ON, snubber capacitor need some amount of power must be stored in the inductor to remove the capacitor energy [7]. To control the OFF and ON of auxiliary and main switch, complementary control gate signals are used. SDCM of operation due to complementary control gate signal scheme, minimum turn on loss of the transistor switch and low diode reverse recovery loss are achieved. So the Null Voltage Resonant Transition (NVRT) of transistor switch is recognized, both turn on and turn off loss is minimized and also eliminates the parasitic ringing in inductor current. This paper describes how to select an inductor for CCM and SDCM of operation, and to select a optimum snubber capacitor, for this a series of MATLAB codes are executed. Finally efficiency comparison between CCM and SDCM of operation is performed and showed that SDCM of operation is the best choice for maximum efficiency and to minimize the size, cost and weight of the converter.

II. CIRCUIT TOPOLOGY

A non-isolated synchronous DC-DC switching power converter technology is used to perform a buck mode of operation. To control the ON and OFF of transistor switches complementary signal gate control scheme is used. The converter is operated in CCM and SDCM of operation. The inductor size, cost and weight of the converter are decreased by SDCM of operation. The SDCM of operation introduces more turn-off loss because of the main switch turn off during more load current [8]. This is one of the drawback of decrease in inductor size. The parasitic ringing of the inductor

current is due to the oscillation of inductor with device output capacitance during turn off period of switch [9]. This issue due to SDCM of operation will affect the efficiency. The turn off loss is minimized by adding snubber capacitor across the transistor switch. The power stored in the capacitor require to be removed before the switch is turned ON for zero turn on loss, thus the snubber capacitor needs some amount of powder must be reserved in the inductor to remove the capacitor energy before the switch is turned ON. Thus the Null Voltage Resonant Transition (NVRT) of transistor switch is recognized. The main advantage of the SDCM of operation is less turn-on loss, so low reverse recovery loss of diode is attained and eliminates the parasitic ringing effect in inductor current. Thus both turn-on and -off losses are minimized. The advantage of CCM of operation is less inductor current ripple, but it increases the inductor volume, converter weight and cost. As a feedback controller PID controller is utilized with inductor current (I*) as a feedback reference [10].

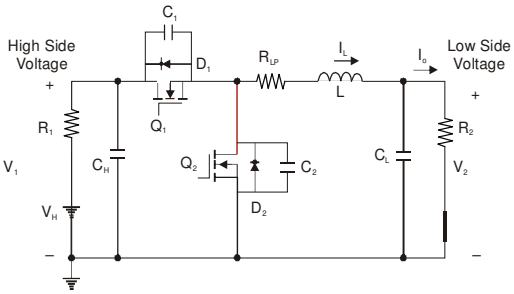

Fig. 1. Circuit topology.

Fig. 1 shows the circuit topology. R_2 acts as load resistance and R_1 is the internal resistance of V_H, which is small as tens of milliohms. The inductor average current (I_L), voltages at high side (V_1) and at low side (V_2) as per state space Eqns. [11] are given in Eqns. (1)-(3).

$$I_L = \frac{D.V_H}{R_1.D^2+R_2+R_p} \quad (1)$$

$$V_1 = \frac{V_H(R_2+R_p)}{R_1.D^2+R_2+R_p} \quad (2)$$

$$V_2 = \frac{D.V_H.R_2}{R_1.D^2+R_2+R_p} \quad (3)$$

where D is the duty cycle given in Eqn. (4)

$$D = \frac{V_H-\sqrt{V_H^2-4(I_L.R_1)(I_L.R_2+I_L.R_P)}}{2(I_L.R_1)} \quad (4)$$

$R_P = R_{dson} + R_{LP}$, R_{dson} is the MOSFET turn-on resistance and R_{LP} is effective series resistance of inductor. Here averaged inductor current is always positive and current flows in one direction. C_H and C_L are the input and output capacitors to smooth the load current and load voltage, its value is 150 µF. Q_1 and Q_2 are MOSFETs with 35 mΩ turn-on resistances, acts as switches with body diode D_1 and D_2 respectively. C_1 and C_2 are snubber capacitors. L is the inductor with effective series resistance R_{LP} of 36 mΩ.

III. INDUCTOR SELECTION

The critical inductor (L_{cr}) value, given in Eqn. (5) [12] permit the converter operate beneath the boundary condition between SDCM and CCM of operation.

$$L_{cr} = \frac{1}{2}.\frac{V_{in}-V_{out}}{P_o}.\frac{V_{out}^2}{V_{in}}.T_s \quad (5)$$

where V_{in} is the input voltage, V_{out} is the output voltage, P_o is output power and T_s is the switching frequency.

The inductor ripple current (ΔI_L) [13] and the inductor conduction loss (P_L) [14] are given in Eqns. (6) and (7) respectively.

$$\Delta I_L = \frac{1}{2}.\frac{V_{in}-V_{out}}{L}.\frac{V_{out}}{V_{in}}.T_s \quad (6)$$

$$P_L = I_{RMS\_L}^2.R_{LP} \quad (7)$$

where R_{LP} is the effective series resistance (ESR) of the inductor L and I_{RMS_L} is the rms inductor current given in Eqn. (8)

$$I_{RMS\_L}^2 = I_L^2 + \frac{\Delta I_L^2}{12} \quad (8)$$

where I_L is the inductor average current.

The different test cases are given in Table 1. A series of MATLAB script are executed, to find minimum inductor value for CCM and SDCM of operation. The results are tabulated in Table 2. The switching frequency considered is 50 KHz. From the Table 2, it is noticed that, the low and high inductor value at border condition is 19.94 µH and 44.42 µH and their corresponding power loss are 15.6 Watt and 8.77 Watt respectively. Therefore the required minimum inductor value to make the converter to operate in SDCM of operation for different test cases must be less than 19.94 µH. Hence 15 µH is considered in circuit topology module which ensures SDCM of operation for different test cases. This inductor conduction loss lies in the range of 12.89 Watt to 19.19 Watt for different test cases in SDCM of operation.

Table 1: Test cases.

Mode of operation	Case	V_H (V)	R_1 (Ω)	R_2 (Ω)	I* (A)	f_{sw} (KHz)
Buck	1	250	10 m	10	15	50
	2	250	10 m	10	20	50
	3	250	10 m	5	20	50
	4	270	10 m	10	15	50

Table 2: Inductor Selection.

Mode of operation	Case*	L_{cr} (µH)	Boundary Condition		SDCM of operation		CCM of operation	
			ΔI_{Lcr} (A)	P_{Lcr} (W)	$\Delta I_{L\text{-}15\mu H}$ (A)	$P_{L\text{-}15\mu H}$ (W)	$\Delta I_{L\text{-}50\mu H}$ (A)	$P_{L\text{-}50\mu H}$ (W)
Buck	1	39.97	15	8.77	39.97	12.89	11.99	8.53
	2	19.94	20	15.60	26.59	16.52	7.97	14.59
	3	29.99	20	15.60	39.99	19.19	11.99	14.83
	4	44.42	15	8.77	44.42	14.02	13.32	8.63

Test cases as in Table 1, for different values of V_H, R_1, R_2, and I

For CCM of operation the required inductor value must be greater than 44.42 µH. Hence 50 µH is considered which ensures CCM of operation for different test cases. This inductor conduction loss lies in the range of 8.53 Watt to 14.83 Watt for different test cases in CCM of operation.

IV. SNUBBER CAPACITOR SELECTION

To minimize the turn-off loss in larger extent, larger value of snubber capacitor is required which minimizes drain current during turn off time, but it leads to large turn on loss, because it will not discharge fully during turn-on period. The snubber capacitor is selected in such a way that it must minimize total turn-on, turn-off and snubber capacitor loss. During switch turn ON time, capacitor voltage fully discharges when the inductor stored power is more than the capacitor power storage capacity. This leads to minimum turn ON loss. The charge balance of CV^2 and $\frac{1}{2}LI_L^2$ is used for snubber capacitor design as given in Eqn. (9) for minimum turn ON loss

$$C.V^2 \leq \frac{1}{2}.L.I_L^2 \quad (9)$$

The above equation is modified for calculation of snubber capacitor value as given in Eqn. (10) which minimizes switching turn on loss as well as snubber capacitor loss.

$$C \leq 0.5.L.\left(\frac{I_L}{V}\right)^2 \quad (10)$$

where C = snubber capacitor, V= capacitor voltage, L= Inductor and I_L = inductor average current.

The power loss in snubber capacitor is given in Eqn. (11) [15]

$$P\_C_{SNU} = \frac{1}{2}.C_s.V_{DS}^2.f_{sw} \quad (11)$$

where C_s is the snubber capacitor, V_{DS} is the maximum voltage across the switch and f_{sw} is the switching frequency

The snubber capacitor is optimized for minimum power loss across it and for minimum switching turn on loss to improve the efficiency. For this, series of MATLAB script are executed and results are tabulated in Table 3. From Eqn. (11) the power loss in snubber capacitor is directly proportional to snubber capacitor value, drain to source voltage of MOSFET and switching frequency, so it is better to select minimum value of snubber capacitor for maximum efficiency. From the Table 3 for SDCM of operation, it is observed that, the minimum snubber capacitor value for maximum capacitor voltage is 23.16 nF and the corresponding power loss through it is 84.37 Watts. To satisfy Eqn. (9), for all different test cases, a snubber capacitor of 22nF is considered in circuit topology module which ensures, the capacitor fully discharge before the switch is turn on, which minimizes the switch turn-on loss.

Table 3: Snubber capacitor selection for SDCM of operation.

Mode of operation	Case*	$V_1=V_{DS}$ (V)	C_{SNU} (nF)	E_C_{SNU} [$C_S.V_1^2$] (Joule)	E_22nf (Joule)	E_15µH [$\frac{1}{2}.L.I_L^2$] (Joule)	P_C_{SNU} (W)	P_22nf (W)
Buck	1	249.90	27.02	0.0017	0.0014	0.0017	84.37	68.70
	2	249.83	48.06	0.003	0.0014	0.003	150	68.66
	3	249.91	48.03	0.003	0.0014	0.003	150	68.70
	4	269.91	23.16	0.0017	0.0016	0.0017	84.37	80.14

Test cases as in Table 1, for different values of V_H, R_1, R_2, and I

Table 4: Snubber Capacitor selection for CCM of operation.

Mode of operation	Case*	$V_1=V_{DS}$ (V)	C_{SNU} (nF)	E_C_{SNU} [$C_S.V_1^2$] (Joule)	E_75nf (Joule)	E_50µH [$\frac{1}{2}.L.I_L^2$] (Joule)	P_C_{SNU} (W)	P_75nf (W)
Buck	1	249.90	90.06	0.0056	0.0047	0.0056	281.25	234.20
	2	249.83	160.21	0.010	0.0047	0.01	500	234.07
	3	249.91	160.10	0.010	0.0047	0.01	500	234.22
	4	269.91	77.20	0.0056	0.0055	0.0056	281.25	273.20

Test cases as in Table 1, for different values of V_H, R_1, R_2, and I

From the Table 4 for CCM of operation, it is observed that, the minimum snubber capacitor value for maximum capacitor voltage is 77.20 nF and the corresponding power loss through it is 281.25 Watts. To satisfy Eqn. (9), for all different test cases, a snubber capacitor of 75nF is considered in circuit topology module which ensures, the capacitor fully discharge before the switch is turn on, which minimizes the switch turn-on loss.

V. EFFICIENCY CALCULATION

Majority of losses in DC-DC switching power converter is from device conduction (MOSFET and diode), switching (MOSFET), inductor and from snubber capacitor. The switch conduction loss and diode conduction loss are given in Eqns. (12) and (13) respectively [8]

$$P_{sw\_con} = I_{sw}\,(0.75+0.003I_{sw}) \quad (12)$$
$$P_{d\_con} = I_d\,(1+0.0016I_d) \quad (13)$$

where I_{sw} and I_d are total switch rms current and total diode rms current respectively, given in Eqns. (14) and (15).

$$I_{sw} = I_{sw\text{-}upper} + I_{sw\text{-}lower} \quad (14)$$
$$I_d = I_{d\text{-}upper} + I_{d\text{-}lower} \quad (15)$$

where $I_{sw\text{-}upper}$ and $I_{sw\text{-}lower}$ are upper and lower switch rms current, given in Eqns. (16) and (17) respectively. $I_{d\text{-}upper}$ and $I_{d\text{-}lower}$ are upper and lower diode rms current, given in Eqns. (18) and (19) respectively.

$$I_{sw-upper} = I_{peak}.\sqrt{\frac{D}{3}} \quad (16)$$

$$I_{sw-lower} = I_{min}.\sqrt{\frac{1-D}{3}} \quad (17)$$

$$I_{d-upper} = I_{min}.\sqrt{\frac{1-D}{3}} \quad (18)$$

$$I_{d-lower} = I_{peak}.\sqrt{\frac{D}{3}} \quad (19)$$

where I_{peak} and I_{min} are inductor peak current and inductor minimum current, given in Eqns. (20) and (21) respectively.

$$I_{peak} = I_L + \Delta I_L \quad (20)$$

$$I_{min} = I_L - \Delta I_L \quad (21)$$

where I_L and ΔI_L are given in equations (1) and (6) respectively

Switching loss in converters occurs during switching transitions and is due to the nonzero multiplication of the MOSFET drain to source current and drain to source voltage and it is given in Eqn. (22) [16]. There is another switching loss due to discharge of drain-to-source capacitor of the MOSFET at the time of turn on; this is given in Eqn. (23) [16].

$$P_{sw1} = \frac{1}{2}.V_{off}.I_{on}.f_{sw}(T_{on} + T_{off}) \quad (22)$$

where V_{off} is the drain-to-source voltage when the switch is off, I_{on} is the drain current when the switch is on and f_{sw} is the switching frequency. The MOSFET on and off times, T_{on} and T_{off} are obtained from data sheets.

$$P_{sw2} = \frac{1}{2}.C_{ds}.V_{off}^2.f_{sw} \quad (23)$$

where C_{ds} is the drain-to-source capacitor of the MOSFET, its value is obtained from datasheet.

The efficiency is calculated by Eqn. (24)

$$\eta = \left[\frac{P_o}{P_o+P_{sw\_con}+P_{d\_con}+P_{sw1}+P_{sw2}+P_L+P\_C_{SNU}}\right] \times 100\% \quad (24)$$

where $P_o = I_o.V_o$, is the output power. I_o and V_o are the output current and output voltage respectively. P_L and P_C_{SNU} are inductor and snubber capacitor loss given in Eqns. (7) and (11) respectively.

VI. EFFICIENCY COMPARISON IN SDCM AND CCM OF OPERATION

Table 5 shows the efficiency comparison among SDCM and CCM of operation for different test cases given in Table 1. From the obtained results, it is noticed that, efficiency in SDCM is more than CCM of operation. But inductor ripple current is more in SDCM of operation than in CCM of operation. Comparison of efficiency and inductor ripple current between SDCM and CCM of operation is shown in Fig. 2.

Table 5: Efficiency in SDCM and CCM of operation.

Mode of operation	Case*	SDCM, L=15 µH				CCM, L=50 µH				η_{diff} (%)
		I_{Peak} (A)	I_{min} (A)	ΔI_L (A)	η (%)	I_{Peak} (A)	I_{min} (A)	ΔI_L (A)	η (%)	
Buck	1	54.97	-24.97	39.97	94.78	26.99	3.00	11.99	89.16	5.62
	2	46.59	-6.59	26.59	96.65	27.97	12.02	7.97	93.28	3.36
	3	59.99	-19.99	39.99	94.03	31.99	8.00	11.99	87.52	6.51
	4	59.42	-29.42	44.42	94.28	28.32	1.67	13.32	87.79	6.49

Test cases as in Table 1, for different values of V_H, R_1, R_2, and I

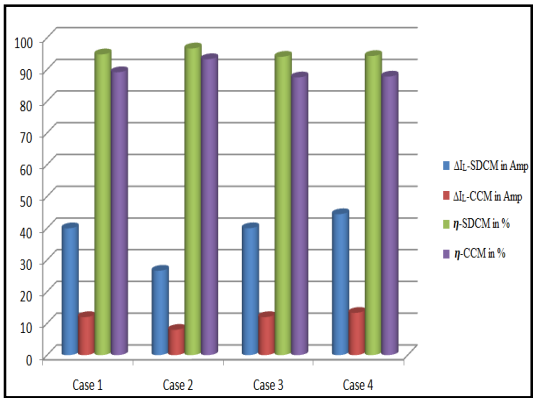

Fig. 2. Variation of inductor ripple current and efficiency.

VII. RESULT AND DISCUSSION

A series of MATLAB script are accomplished to determine the optimum value of snubber capacitor and inductor based on the low device and switch conduction loss condition to improve the efficiency. From the obtained result 15 µH and 50 µH is considered as optimum inductors for SDCM and CCM of operation, and 22nf and 75nf is considered as optimum snubber capacitor for SDCM and CCM of operation respectively. Efficiency range of 94.03 % to 96.65 % in SDCM of operation and 87.52 % to 93.28 % in CCM of operation is obtained for different test case. Compared with fuzzy based interleaved DC-DC buck converter [17] , the proposed converter have better efficiency and also decrease in volume, cost and weight of the converter.

VIII. CONCLUSION

The paper describes a more efficient synchronous non-isolated buck DC-DC switching power converter. The converter is made to operate in Synchronous Discontinuous Current Mode (SDCM) and Continuous Current Mode (CCM) of operation. A series of MATLAB script are accomplished to identify the snubber capacitor and inductor value for SDCM and CCM of operation. A complementary signal gate control technique is applied to turn off and on the MOSFET switch. Anti-parallel diode of the MOSFET switch helps to discharge the capacitor. Efficiency in SDCM and CCM of operations for different test cases is carried out. From the obtained result, it is observed that, the efficiency is more in SDCM of operation than in CCM of operation. So, SDCM of operation is the best choice for maximum efficiency and to minimize the size, cost and weight of the converter.

It is possible to improve the efficiency by introducing some soft switching cell to the topology is the future scope.

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How to cite this article: Mahesh Gowda N. M. (2019). Efficiency of Buck DC-DC Switching Power Converter in CCM and SDCM of Operation. *International Journal on Emerging Technologies*, *10*(4): 354–358.